Remarks

This Preliminary Amendment is being used to add the parentage of the present application and reduce the number of pending claims from the original application in order to reduce the filing fee. An Information Disclosure Statement is also being filed to include references cited in the parents to the present application as well as several additional references that have subsequently become know to the applicants.

EXPRESS MAIL LABEL NO:

EV 321718356 US

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APPENDIX

Pending claims

1. A multi-state memory comprising:

a plurality of multi-state memory cells, each for storing one of a plurality of N multi-states;

at least one plurality of M populations of tracking cells, wherein each of said populations is associated with one of said multi-states, and wherein M is less than N; and

a read circuit for reading said multi-state memory cells using read points for each of said plurality of multi-states based upon the threshold voltages associated with the programmed state of said populations of tracking cells.

2. The multi-state memory of claim 1, wherein said memory cells are organized into a plurality of sectors, wherein each of said sectors has an associated plurality of M populations of tracking cells and a corresponding set of read points.

3. The multi-state memory of claim 2 further comprising a plurality of cells storing error correction code associated with each of said sectors.

4. The multi-state memory of claim 2, further comprising:

a programming circuit for writing data values to said memory cells and for programming said tracking cells.

5. The multi-state memory of claim 4, wherein said programming circuit includes a verify circuit using a set of fixed reference values for program verify for writing data values to said memory cells and the same set of fixed reference values for program verify for programming said tracking cells.

6. The multi-state memory of claim 5, wherein a tracking cell which fails to be verified by the verify circuit when programming said tracking cells is removed from said populations of tracking cells.

7. The multi-state memory of claim 5, wherein said programming circuit writes said memory cells and programs said tracking cells within a sector concurrently.

8. The multi-state memory of claim 1, wherein said read circuit comprises:

tracking cell read circuitry for reading threshold voltages associated with the programmed state of said tracking cells;

a memory controller for establishing the read points for each of said plurality of multi-states based upon said threshold voltages read from said populations of tracking cells.

9. The multi-state memory of claim 8, wherein said memory controller further manages the multi-state memory and transfers data between the memory and a host system to which it is connected.

10. The multi-state memory of claim 8, wherein said memory controller forms part of the same integrated circuit as said memory cells and said populations of cells tracking cells.

11. The multi-state memory of claim 8, wherein said memory controller forms part of an integrated circuit separate from said memory cells and said populations of cells tracking cells.

12. The multi-state memory of claim 11, wherein said read circuit further comprises:

a fast look-up table for storing said the read points established by said memory controller, wherein the fast look-up table forms part of the same integrated circuit as said memory cells and said populations of cells tracking cells, and wherein the multi-state memory cells are read using the fast look-up table.

13. The multi-state memory of claim 1, wherein each of said populations of tracking cells comprises a plurality of tracking cells.

14. The multi-state memory of claim 13, wherein M is equal to two.

Claims 15-129 have been cancelled.